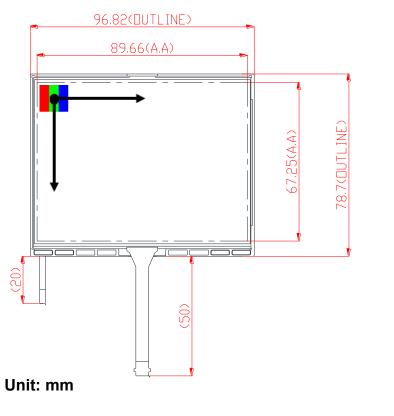
# GTC Thank You!

**Great Tech Corporation - http://www.gtc-tw.com/gtc.htm** Mobile: +886-928083208 - Wack Lin, wacklink@gtc-tw.com Tel: +886-2-8211-1330 - Lily Ko, lily@gtc-tw.com No.120, DingCheng 3rd Street., XinDian Dist., New Taipei City 23153, Taiwan

# 4.4" MIP Reflective Color LTPS TFT LCD with Back Light TX11D200VM1AAA

# Features:

- Ultra low power consumption
- 8 colors, SPI I/F
- Super high reflectance 18%
- Slim & compact design



	<u>MP now</u>		Spec		
		LCD type	ECB, Full Reflective		
		Diagonal size	4.4"		
	General	Resolution	640RGBx480		
	General	Active area	89.664mm(H) x 67.248mm(V)		
		Pixel Pitch	46.7um(H)(Ave.) x 140.1um(V)		
		PPI	181.3		
-		Interface (Note-1)	SPI Max refresh frequency (2) Hz		
	Electrical	Power Supply	VLCD=3V		
		Power Consumption (except B/L) (Note-2)	Typ. 14μW @ MIP Static Image Typ. 123μW @MIP 1fps Image Typ. (250μW) @MIP 2fps Image Refresh		
		Color gamut	Typ. 23% (NTSC ratio)		
	Optical	Contrast ratio	Тур.40:1		
	@Reflective mode	Number of colors	8 (1bit)		
		Reflectance	18%		
		Glass size	92.664mm(H) x 72.748mm(V) x 1.0mm(T)		
	Mechanical	Module structure	LCD panel + FPC + BL		
		Module dimensions	96.82mm(H) x 78.7mm(V) x 3mm(D)		
	Feature	Feature	Memory In Pixel		
	Top/Tst		-20~70/-30~80		

Note-1: Room Temperature, 3V drive Note-2: Room Temperature, White Image

# Color reflective LCD

# 4.4-inch - TX11D200VM1AAA

This LCD modules are suitable for a wide variety of IoT products and application, including outdoor sports gears, medical & healthcare devices, remote controllers, and portable devices due to key features.

# Ultra-Low Power Consumption

Long battery life with JDI's original technology.

# **User-friendly I/F**

SPI/ 3V Drive



# **Good Outdoor Visibility**

Good visibility realized by proprietary reflective color technology.

# **High Display Quality**

Excellent image quality with high color reflectance

Features	1.28"	2.7"	4.4"
LCD type	ECB, Reflective	ECB, Reflective	ECB, Reflective
Resolution	176x176	400x240	640x480
Interface	SPI	←	←
Contrast	Typ. 30:1	Typ.(40:1)	←
No. of colors	8 colors	←	←
Color gamut (NTSC ratio)	23%	←	<i>←</i>
Reflectance	26%	19%	18%
Viewing angle (L/R/T/B, CR>2)	(60)/(65)/(65)/(60)	(70)/(70)/(70)/(70)	(70)/(70)/(70)/(70)

0 0 (	<pre></pre>		V - 7 V - 7 V - 7 V - 7
Backlight	Optional	Vec	Vec
Dackiight	Optional	165	165

# **Software Development Kit**

Open source software is available at Mbed OS site (<u>https://os.mbed.com/teams/JapanDisplayInc/</u>)



Kaohsiung Opto-Electronics Inc.

FOR MESSRS : \_\_\_\_\_

DATE : Jun. 21<sup>st</sup>,2018

# CUSTOMER'S ACCEPTANCE SPECIFICATIONS

# TX11D200VM1AAA

### Contents

No.         ITEM         SHEET No.         PAGE           1         COVER         7B64PS 2701-TX11D200VM1AAA-2         1-1/1           2         RECORD OF REVISION         7B64PS 2702-TX11D200VM1AAA-2         2-1/1           3         GENERAL DATA         7B64PS 2703-TX11D200VM1AAA-2         2-1/1           4         ABSOLUTE MAXIMUM RATINGS         7B64PS 2704-TX11D200VM1AAA-2         3-1/1           5         ELECTRICAL CHARACTERISTICS         7B64PS 2704-TX11D200VM1AAA-2         5-1/1           6         OPTICAL CHARACTERISTICS         7B64PS 2706-TX11D200VM1AAA-2         5-1/1           6         OPTICAL CHARACTERISTICS         7B64PS 2707-TX11D200VM1AAA-2         6-1/3~3/3           7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         6-1/3~3/3           7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         8-1/1           9         LCD INTERFACE         7B64PS 2709-TX11D200VM1AAA-2         8-1/1           9         LCD INTERFACE         7B64PS 2710-TX11D200VM1AAA-2         9-1/19~19/19           10         OUTLINE DIMENSIONS         7B64PS 2711-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         11-1/3~3/3           12         PRECAUTIONS				
2         RECORD OF REVISION         7B64PS 2702-TX11D200VM1AAA-2         2-1/1           3         GENERAL DATA         7B64PS 2703-TX11D200VM1AAA-2         3-1/1           4         ABSOLUTE MAXIMUM RATINGS         7B64PS 2704-TX11D200VM1AAA-2         4-1/1           5         ELECTRICAL CHARACTERISTICS         7B64PS 2705-TX11D200VM1AAA-2         5-1/1           6         OPTICAL CHARACTERISTICS         7B64PS 2706-TX11D200VM1AAA-2         6-1/3~3/3           7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         6-1/3~3/3           7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         6-1/3~3/3           7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         6-1/3~3/3           9         LCD INTERFACE         7B64PS 2708-TX11D200VM1AAA-2         8-1/1           9         LCD INTERFACE         7B64PS 2709-TX11D200VM1AAA-2         9-1/19~19/19           10         OUTLINE DIMENSIONS         7B64PS 2710-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         11-1/3~3/3           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	No.	ITEM	SHEET No.	PAGE
3         GENERAL DATA         7B64PS 2703-TX11D200VM1AAA-2         3-1/1           4         ABSOLUTE MAXIMUM RATINGS         7B64PS 2704-TX11D200VM1AAA-2         4-1/1           5         ELECTRICAL CHARACTERISTICS         7B64PS 2705-TX11D200VM1AAA-2         5-1/1           6         OPTICAL CHARACTERISTICS         7B64PS 2706-TX11D200VM1AAA-2         6-1/3~3/3           7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         7-1/1           8         RELIABILITY TESTS         7B64PS 2708-TX11D200VM1AAA-2         8-1/1           9         LCD INTERFACE         7B64PS 2709-TX11D200VM1AAA-2         9-1/19~19/19           10         OUTLINE DIMENSIONS         7B64PS 2710-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         10-1/1           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	1	COVER	7B64PS 2701-TX11D200VM1AAA-2	1-1/1
4         ABSOLUTE MAXIMUM RATINGS         7B64PS 2704-TX11D200VM1AAA-2         4-1/1           5         ELECTRICAL CHARACTERISTICS         7B64PS 2705-TX11D200VM1AAA-2         5-1/1           6         OPTICAL CHARACTERISTICS         7B64PS 2706-TX11D200VM1AAA-2         6-1/3~3/3           7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         7-1/1           8         RELIABILITY TESTS         7B64PS 2708-TX11D200VM1AAA-2         8-1/1           9         LCD INTERFACE         7B64PS 2709-TX11D200VM1AAA-2         9-1/19~19/19           10         OUTLINE DIMENSIONS         7B64PS 2710-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         10-1/1           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	2	RECORD OF REVISION	7B64PS 2702-TX11D200VM1AAA-2	2-1/1
5         ELECTRICAL CHARACTERISTICS         7B64PS 2705-TX11D200VM1AAA-2         5-1/1           6         OPTICAL CHARACTERISTICS         7B64PS 2706-TX11D200VM1AAA-2         6-1/3~3/3           7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         7-1/1           8         RELIABILITY TESTS         7B64PS 2708-TX11D200VM1AAA-2         8-1/1           9         LCD INTERFACE         7B64PS 2709-TX11D200VM1AAA-2         9-1/19~19/19           10         OUTLINE DIMENSIONS         7B64PS 2710-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         11-1/3~3/3           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	3	GENERAL DATA	7B64PS 2703-TX11D200VM1AAA-2	3-1/1
6         OPTICAL CHARACTERISTICS         7B64PS 2706-TX11D200VM1AAA-2         6-1/3~3/3           7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         7-1/1           8         RELIABILITY TESTS         7B64PS 2708-TX11D200VM1AAA-2         8-1/1           9         LCD INTERFACE         7B64PS 2709-TX11D200VM1AAA-2         9-1/19~19/19           10         OUTLINE DIMENSIONS         7B64PS 2710-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         11-1/3~3/3           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	4	ABSOLUTE MAXIMUM RATINGS	7B64PS 2704-TX11D200VM1AAA-2	4-1/1
7         BLOCK DIAGRAM         7B64PS 2707-TX11D200VM1AAA-2         7-1/1           8         RELIABILITY TESTS         7B64PS 2708-TX11D200VM1AAA-2         8-1/1           9         LCD INTERFACE         7B64PS 2709-TX11D200VM1AAA-2         9-1/19~19/19           10         OUTLINE DIMENSIONS         7B64PS 2710-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         11-1/3~3/3           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	5	ELECTRICAL CHARACTERISTICS	7B64PS 2705-TX11D200VM1AAA-2	5-1/1
8         RELIABILITY TESTS         7B64PS 2708-TX11D200VM1AAA-2         8-1/1           9         LCD INTERFACE         7B64PS 2709-TX11D200VM1AAA-2         9-1/19~19/19           10         OUTLINE DIMENSIONS         7B64PS 2710-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         11-1/3~3/3           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	6	OPTICAL CHARACTERISTICS	7B64PS 2706-TX11D200VM1AAA-2	6-1/3~3/3
9         LCD INTERFACE         7B64PS 2709-TX11D200VM1AAA-2         9-1/19~19/19           10         OUTLINE DIMENSIONS         7B64PS 2710-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         11-1/3~3/3           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	7	BLOCK DIAGRAM	7B64PS 2707-TX11D200VM1AAA-2	7-1/1
10         OUTLINE DIMENSIONS         7B64PS 2710-TX11D200VM1AAA-2         10-1/1           11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         11-1/3~3/3           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	8	RELIABILITY TESTS	7B64PS 2708-TX11D200VM1AAA-2	8-1/1
11         APPEARANCE STANDARD         7B64PS 2711-TX11D200VM1AAA-2         11-1/3~3/3           12         PRECAUTIONS         7B64PS 2712-TX11D200VM1AAA-2         12-1/2~2/2	9	LCD INTERFACE	7B64PS 2709-TX11D200VM1AAA-2	9-1/19~19/19
12 PRECAUTIONS 7B64PS 2712-TX11D200VM1AAA-2 12-1/2~2/2	10	OUTLINE DIMENSIONS	7B64PS 2710-TX11D200VM1AAA-2	10-1/1
	11	APPEARANCE STANDARD	7B64PS 2711-TX11D200VM1AAA-2	11-1/3~3/3
13 DESIGNATION OF LOT MARK 7B64PS 2713-TX11D200VM1AAA-2 13-1/1	12	PRECAUTIONS	7B64PS 2712-TX11D200VM1AAA-2	12-1/2~2/2
	13	DESIGNATION OF LOT MARK	7B64PS 2713-TX11D200VM1AAA-2	13-1/1

ACCEPTED BY:

PAGE 1-1/1

2. RECORD OF REVISION						
DATE	SHEET No.	SUMMARY				
Jun.21,'18	7B64PS-2703- TX11D200VM1AAA-2 Page 3-1/1	3.1 DISPLAY FEATURES Revised : Power Consumption : 0.153 W for LCD $\rightarrow$ 0.005	54 W for LCD			
KAOHSIUNG	G OPTO-ELECTRONICS	NC. SHEET 7B64PS 2702-TX11D200VM	1AAA-2 PA	GE	2-1/1	

# 3. GENERAL DATA

### **3.1 DISPLAY FEATURES**

This module is a 4.4" VGA of 4:3 format of LTPS(Lower temperature Poly-Silicon) TFT. The pixel format is vertical stripe and sub pixels are arranged as R(red), G(green), B(blue) sequentially .This display is RoHS compliant , and LED backlight are applied on this display.

Part Name	TX11D200VM1AAA
Module Dimensions	96.82(W) mm x 78.7(H) mm x 3.0(D) mm
LCD Active Area	89.664(W) mm x 67.248(H) mm
Pixel Pitch	0.140(W) mm x 0.140(H) mm
Resolution	640 x 3(RGB)(W) x 480(H) Dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Reflective color TFT; Normal Black
Display Type	Active Matrix
Number of Colors	8 Colors
Backlight	Light Emitting Diode (LED)
Weight	30g
Interface	SPI ; 10 pins
Power Supply Voltage	3.3V for LCD; 3.3V for Backlight
Power Consumption	0.0054 W for LCD ;0.396W for backlight
Feature	MIP(Memory in pixel) Reflective type LCD
Polarizer	Hard Coat type (*Pencil Hardness : 2H)

# 4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage for Analog	$V_{\text{DDA}}$	-0.3	3.6	V	-
Supply Voltage for Logic	V <sub>DD</sub>	-0.3	3.6	V	-
Input Voltage of Logic	VI	V <sub>SS</sub> -0.3	3.6	V	-
Operating Temperature	T <sub>op</sub>	-20	70	°C	Note 1
Storage Temperature	T <sub>st</sub>	-30	80	°C	Note 1
Backlight Input Voltage	$V_{BL+}$	0	4	V	-
LED forward current	I <sub>F</sub>	-	30	mA	Note 2
LED Pulse Forward current	I <sub>FP</sub>	-	100	mA	Note 3

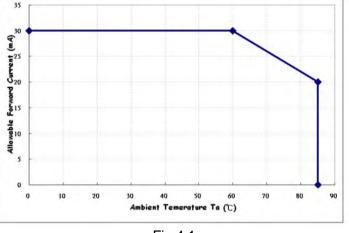
Note 1: The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Optical performances and response time would be different in temperatures other than 25  $^\circ C$  .

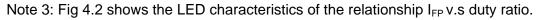
- Operating under high temperature will shorten LED lifetime.

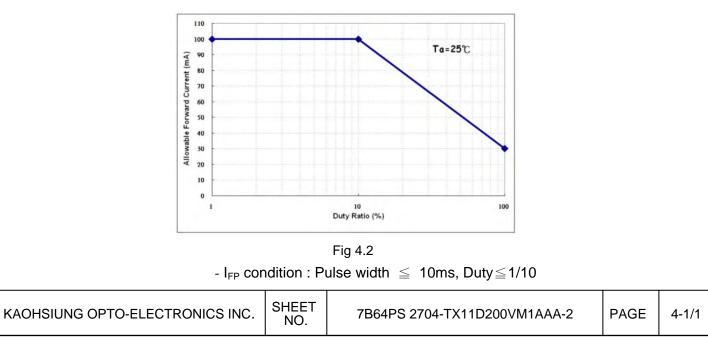


Note 2: Fig 4.1 shows the maximum rating of forward current based on different temperature.









# **5. ELECTRICAL CHARACTERISTICS**

### 5.1 LCD CHARACTERISTICS

5.1 LCD CHARACTERISTICS $T_a = 25 \degree C, \ Vss = 0V$							
ltem		Symbol	Min.	Тур.	Max.	Unit	Remarks
	Analog	$V_{\text{DDA}}$	2.7	3.0	3.6		-
	Analog	V <sub>SSA</sub>	-	0	-		-
Power Supply Voltage	Logic	$V_{DD}$	2.7	3.0	3.6		Note 1
	LOGIC	$V_{SS}$	-	0	-	v	Note 2
Innut Cirnal Valtage	Hi	V <sub>IH</sub>	V <sub>DD</sub> -0.1	$V_{DD}$	$V_{DD}$		Nata 2
Input Signal Voltage	Low	V <sub>IL</sub>	$V_{SS}$	$V_{SS}$	V <sub>SS</sub> +0.1		Note 3
Power Supply Current	-	IDD	-	1.8	2.5	mA	Note 4

Note 1: Apply to EXTMODE = "H".

Note 2: Apply to EXTMODE = "L".

Note 3: Apply to SCLK, SI, SCS, DISP, EXTCOMIN.

Note 4: Data update frequency=1Hz, fCOM frequency=60Hz, test pattern by "All White".

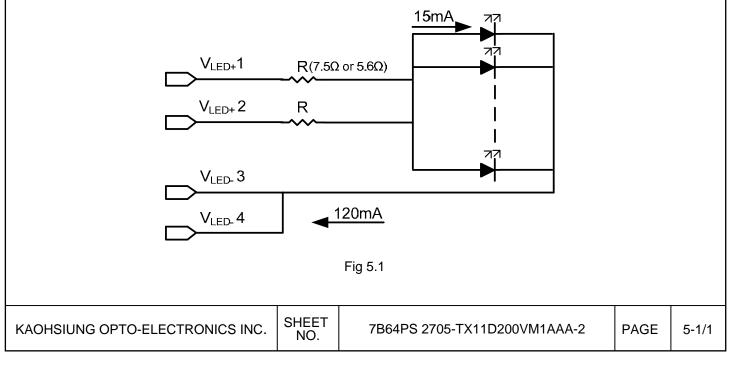
### 5.2 BACKLIGHT CHARACTERISTICS

							$I_a = 25$ C
Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Remarks
LED Input Voltage	$V_{\text{LED}}$	-	3.0	3.3	3.6	V	Note1
LED Forward Current	I <sub>LED</sub>	-	-	120	-	mA	Note2
LED lifetime	-	I <sub>LED</sub> =120 mA	-	50K	-	hrs	-

 $T = 25 \ ^{\circ}C$ 

Note 1: As Fig. 5.1 shown the LED backlight circuit, VLED and ILED is many to one relationship, the above V<sub>LED</sub> range is defined to obtain 120 mA.

Note 2: Estimated lifetime is specified as the time to reduce 50% brightness by applying 120 mA.



# 6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 20 minutes.
- The ambient temperature is  $25\pm5\,^{\circ}C\,.$
- In the dark room less than 100lx, the equipment has been set for the measurements as shown in Fig 6.1 and Fig 6.3.

For reflection mode

						$T_a = 25 \ ^\circ C, V_a$	DD = 3.0V
lien				Rating			Demorte
Item	Symbol	Temp.(°C)	Min.	Тур.	Max.	Unit	Remark
Contrast	CR	25	20	40	-	-	Note 1
Desperance	tr	05	-	4	8		Nata 0
Response	tf	25	-	6	12	ms	Note 2
	Rx		-	0.51	-		
	Ry		-	0.32	-		
	Gx		-	0.30	-		
Color	Gy		-	0.45	-	-	Note 3
Coordinates	Bx	25	-	0.16	-		
	Ву		-	0.18	-		
	Wx		-	0.30	-		
	Wy		-	0.33	-		
NTSC ratio	-	25	-	23	-	%	Note 4
Reflectance	-	25	10	18	-	%	-
	θL	25	55	70	-		
Viewing Angle	θR		55	70	-	0	Nata 5
(CR>2)	θΤ		55	70	-	]	Note 5
	θB		55	70	-		

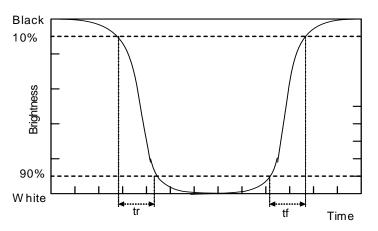
### For transmission mode

 $T_a = 25 \ ^{\circ}C, V_{DD} = 3.0V$ 

Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Remarks
Brightness of White	В	I <sub>BL</sub> =120mA	8	10	-	cd/m <sup>2</sup>	Note 7
Brightness Uniformity	-	-	70	-	-	%	Note 8

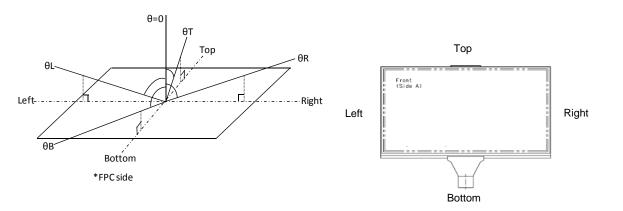
Note 1: This is a ratio between the screen surface reflectance of the white raster and the black raster

- $CR = \frac{Reflection intensity on all pixels White}{Reflection intensity on all pixels Black}$
- Note 2: The response time is defined as the following figure and shall be measured by matching the input signal for "Black" and "White".
  - Normally Black mode



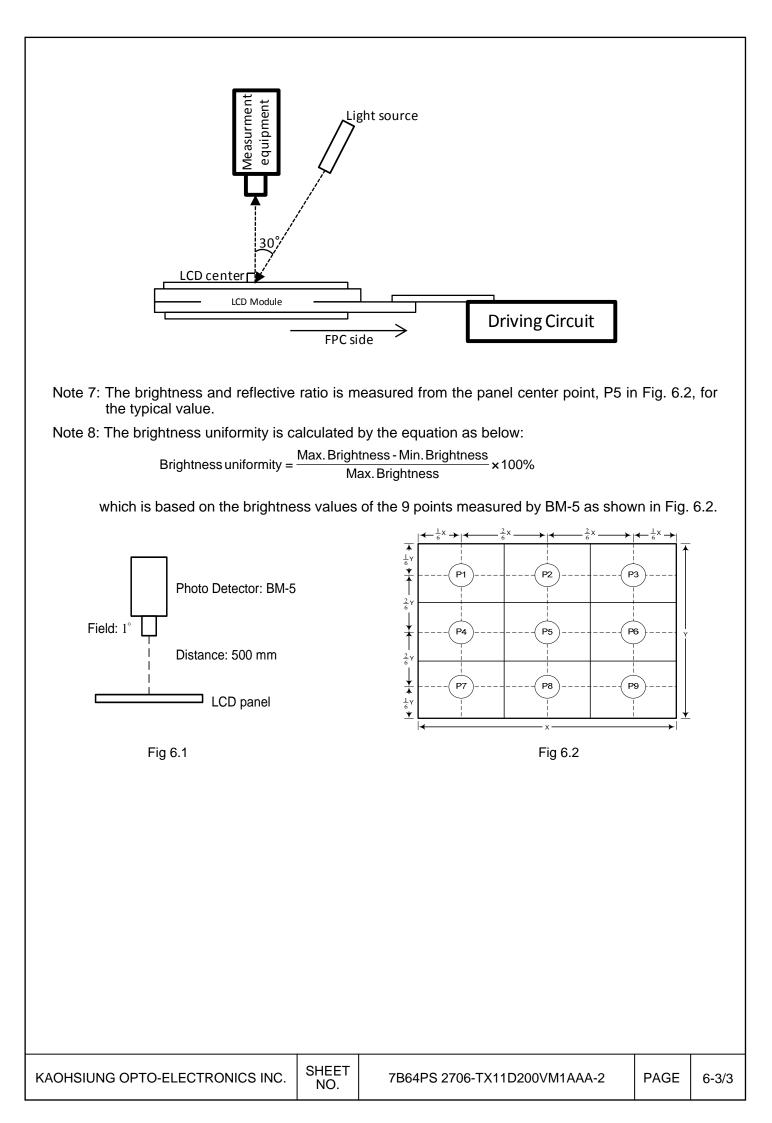
- tr: Response time from Black to White
- tf: Response time from White to Black

- Note 3: This is the x-y coordinate of Red, Green, Blue and White colors specified on the CIE1931 chromaticity diagram. (\* It is not a guaranteed value)
- Note 4: This is an area of a triangle shaped by R, G and B coordinates on the CIE1931 chromaticity diagram.
- Note 5: This is a maximum angle  $\theta$  from the normal direction that keeps having the contrast more than 2.

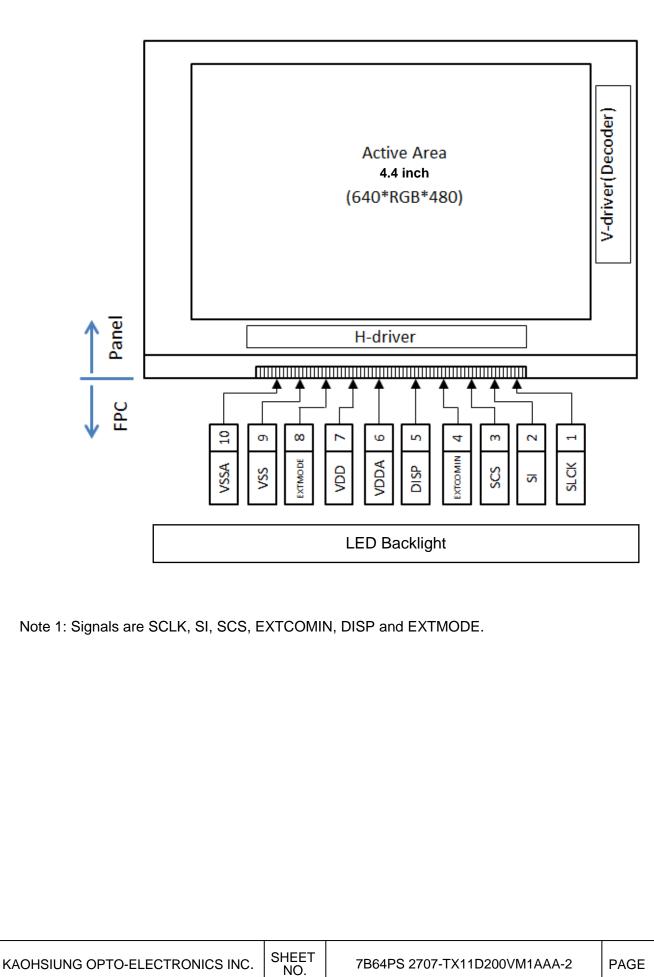


Note 6: Measurement system-for reflective mode

- Light source: Parallel light source
- D65 / 2 degree viewing angle
- Light source input direction : from opposite side of FPC side (30°)
- Light source receive direction : at LCD center (0°)



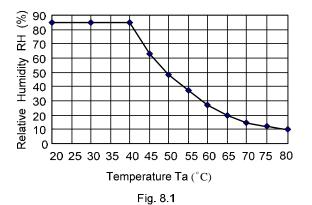
# 7. BLOCK DIAGRAM



# 8. RELIABILITY TESTS

Test Item	Condition	
High Temperature	1) Operating 2) 70°C	240 hrs
Low Temperature	1) Operating 2) -20℃	240hrs
High Temperature	1) Storage 2) 80°C	240 hrs
Low Temperature	1) Storage 2) -30℃	240 hrs
Thermal Shock	1) Non-Operating 2) -35°C ↔ 85°C 3) 0.5 hr ↔ 0.5 hr	240 hrs
High Temperature & Humidity	1) Operating 2) 40°C & 85%RH 3) Without condensation	240 hrs (Note 3)
Mechanical Shock	1) Non-Operating 2) 10 ms 3) 50G 4) $\pm X$ , $\pm Y$ and $\pm Z$ directions	Once for each direction
ESD	1) Operating 2) Tip: 150 pF, 330 $\Omega$ 3) Contact discharge for glass: ± 1KV 4) R=1.5k $\Omega$ , C=100pF	1) Glass: 9 points (Note 4)

- Note 1: Display functionalities are inspected under the conditions defined in the specification after the reliability tests.
- Note 2: The display is not guaranteed for use in corrosive gas environments.
- Note 3: Under the condition of high temperature & humidity, if the temperature is higher than 40°C, the humidity needs to be reduced as Fig. 8.1 shown.



Note 4: All pins of LCD interface (CN1) have been tested by ±100V contact discharge of ESD under non-operating condition.

# 9. LCD INTERFACE

### 9.1 INTERFACE PIN CONNECTIONS

CN1 pin assignment of LCD interface is as below:

Pin No.	Symbol	Function	Remark
1	SCLK	Serial Clock Signal	
2	SI	Serial Data Input Signal	
3	SCS	Chip Select Signal	
4	EXTCOMIN	COM Inversion Signal Input	
5	DISP	Display ON/OFF Switching Signal	Note 1
6	$V_{DDA}$	Power Supply for Analog	
7	V <sub>DD</sub>	Power Supply for Logic	
8	EXTMODE	COM Inversion Mode Select Terminal	Note 2
9	$V_{SS}$	Logic Ground	
10	$V_{SSA}$	Analog Ground	

Note 1: ON/OFF signal is only for display. Data memory is kept also at the time of on/off.

"H" : Data memory will be displayed.

"L" : Solid black color will be displayed and data memory will be saved.

Note 2: "H": Enable EXTCOMIN signal, connect to  $V_{\text{DD}}$ .

"L": Enable serial input flag, connect to  $V_{SS}$ .

CN2 pin assignment of Backlight is as below:

Pin No.	Signal	Level	Function
1	$V_{LED}$ +	-	Power Supply for LED
2	V <sub>LED</sub> +	-	Power Supply for LED
3	V <sub>LED</sub> -	-	GND
4	V <sub>LED</sub> -	-	GND

### 9.2 RECOMMENDED CIRCUIT

	No.	Symbol
	1	SCLK
	2	SI
	3	SCS
	4	EXTCOMIN
	5	DISP
	6	V <sub>DDA</sub>
	7	V <sub>DD</sub>
	8	EXTMODE
<b> </b>	9	V <sub>SS</sub> V <sub>SSA</sub>
	10	V <sub>SSA</sub>

EXTMODE=L : COM Signal Serial Input EXTMODE=H : COM Signal External Input

	No.	Symbol
	1	SCLK
	2	SI
	3	SCS
	4	EXTCOMIN
	5	DISP
	6	V <sub>DDA</sub>
	7	V <sub>DD</sub>
L	8	EXTMODE
	9	V <sub>SS</sub> V <sub>SSA</sub>
	10	V <sub>SSA</sub>

### External circuit example

	No.	symbol
<u></u>	1	SCLK
C1:0.1uF/B/10V	2	SI
C2:0.1uF/B/10V C3:1.0uF/B/10V	3	SCS
C3.1.001/16/10v	4	EXTCOMIN
•	5	DISP
	6	VDDA
+ + +	7	VDD
$\pm c_1 \pm c_2 \pm c_3 - \cdots$	8	EXTMODE
<b>→   →</b>	9	VSS
<b>\</b>	10	VSSA

### 9.3 INPUT SIGNAL CHARACTERISTICS

Ta=25°C. Driving Condition : VI	DD=3.0V,VDDA=3.0V,VIH=3.0V,VIL=0V

					<del>т т</del>	
PARAMETER	SYMBOL	Min.	Тур.	Max.	UNIT	REMARKS
Clock frequency	fSCLK	-	1.00	2.00	MHz	Note1
COM frequency	fCOM	50	60	-	Hz	Note2
SCS rising time	trSCS	-	-	50	ns	
SCS falling time	tfSCS	-	-	50	ns	
SCS Low width	twSCSL	6.0	-	-	us	
SCS settling time	tsSCS	6.0	-	-	us	
SCS holding time	thSCS	2.0	-	-	us	Note3
SI rising time	trSI	-	-	50	ns	
SI falling time	tfSI	-	-	50	ns	
SI settling time	tsSI	200	450	-	ns	
SI holding time	thSI	250	500	-	ns	
SCLK rising time	trSCLK	-	-	50	ns	
SCLK falling time	tfSCLK	-	-	50	ns	
SCLK High width	twSCLKH	250	500	-	ns	Note4
SCLK Low width	twSCLKL	250	500	-	ns	Note4
EXTCOMIN frequency	fXTCOMIN	1	-	140	Hz	
EXTCOMIN rising time	trEXTCOMIN	-	-	50	ns	
EXTCOMIN falling time	tfEXTCOMIN	-	-	50	ns	
EXTCOMIN High width	twEXTCOMIN	2.0	-	-	us	
DISP rising time	trDISP	-	-	50	ns	
DISP falling time	tfDISP	-	-	50	ns	

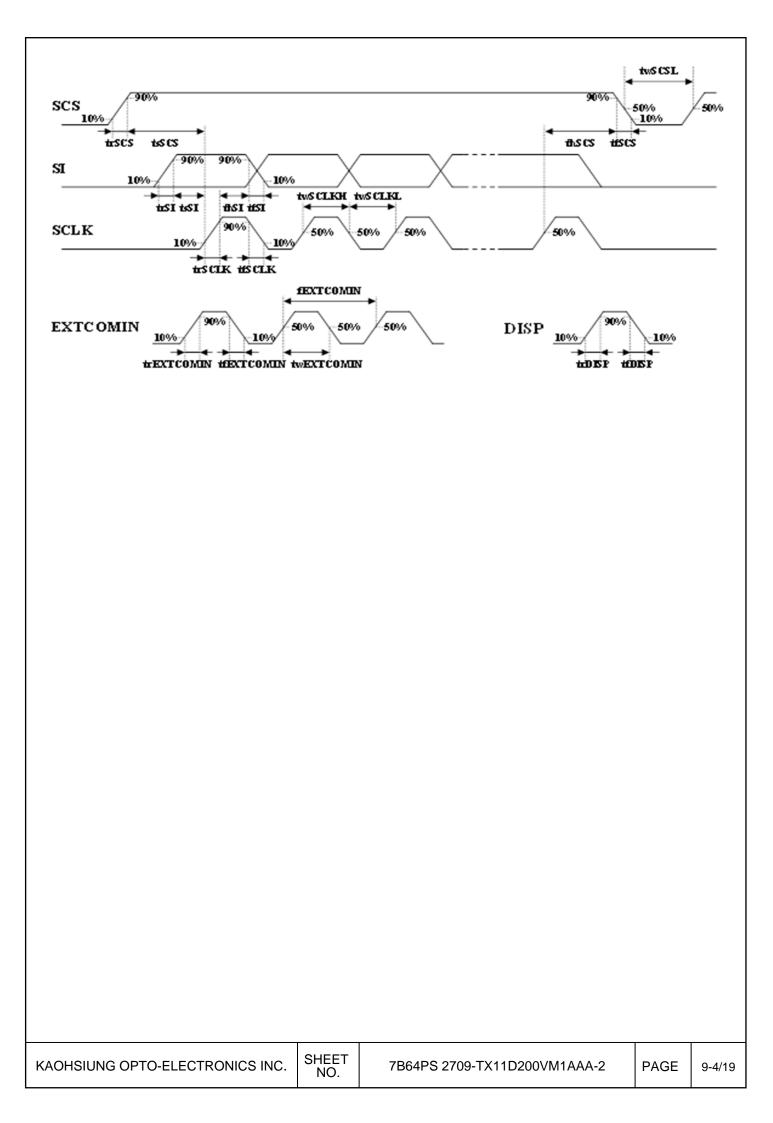
Note 1: Please note that Max. fSCLK may be lowered when VDD and VDDA fall than 3.0V at a low temperature.

Note 2: COM frequency should be around 60Hz for transmissive mode.

ex: For Data update mode M2 level must be reversed per 8 gate lines based on fSCLK =1MHz.

Note 3: In the case of data update mode in transmissive mode, thSCS should be 50us or less.

Note 4: twSCLKH and twSCLKL should be approximately the same length, if possible.



### 9.4 POWER ON/OFF SEQUENCE

	}	-	On see	quence		Normal operation	Off sequence		
			T2	T3	T4		T5 T6 T7		
DD/VDDA	GND	/		(*45)	(*45)				
DISP	GND								
XTCOMIN	GND					Normal Operation			
CS	GND		(*46)	1		Normal Operation	(*46)		
CLK/SI	GND	_	(*46)			Normal Operation	(*46)		

[On sequence]

- T1 : Power supply rising time. (Depends on external power supply)
- T2 : Pixel memory initialization 1ms or more initialize with M2 (all clear flag)
- T3 : Release time for internal latch circuits. 30us or more
- T4 : COM polarity initialization time. 30us or more

[Normal operation] Duration of normal operation

[Off sequence]

- T5 : Pixel memory initialization. Same as T2.
- T6 : COM and latch circuits initialization. 30us or more
- T7 : Power supply falling time. (Depends on external power supply)

\*Refer to the timing chart and electrical characteristics for details.

Note 5: It is allowed to replace T3 and T4 mutually.

In the case of starting EXTCOMIN before rising DISP, EXTCOMIN is ignored during DISP="L". Also, it is allowed to start simultaneously DISP and EXTCOMIN.

In that case, it is necessary to insert 100us or more (200us or less) before normal operation.

### Note 6: Pixel memory initialization.

Use M2 (all clear flag : refer to 6.8),

or write black data to all pixel memories (refer to the data update mode).

[Remark]

VDD and VDDA should rise simultaneously or VDD should rise first.

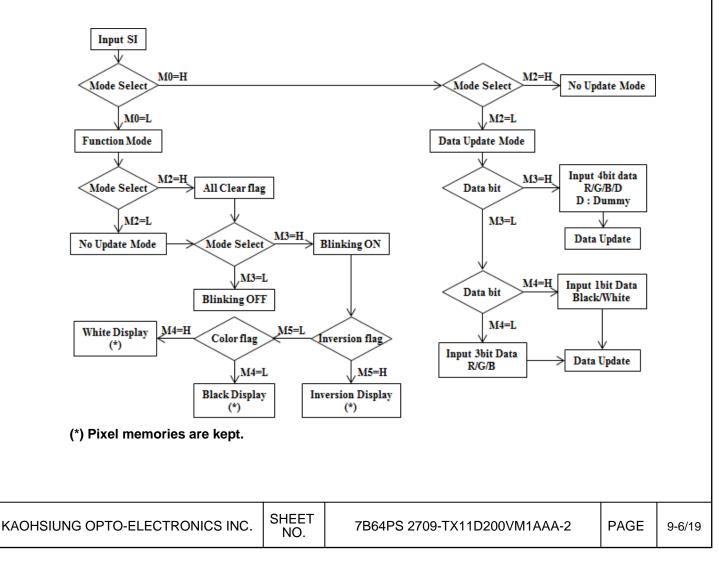
VDD and VDDA should fall simultaneously or VDDA should fall first.

### 9.5 Mode

### 9.5.1 MODE TABLE

Mode select Unassigned bit and AG9-8 : No care, it can be H or L (L is Recommended)											mmended)						
	M0	M1	M2	M3	M4	M5	AG9	AG8	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0	Mode
	L	L/H	L	L	-	-	-	-	-	-	-	-	-	-	-	-	No-Update
	L	L/H	L	H	L/H	L/H	-	-	-	-	-	-	-	-	-	-	Blinking
	L	L/H	H	L/H	L/H	L/H	-	-	-	-	-	-	-	-	-	-	All Clear
	H	L/H	L	L/H	L/H	-	AG9	AG8	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0	Data-Update
	H	L/H	H	L/H	L/H	L/H	-	-	-	-	-	-	-	-	-	-	No-Update
Mode (6bit) Gate Address (10bit) Function table																	
	M0-	Lorl	MU-H	/ML2=1	1			_	MU=F	I/M2=	L						
		Mo	de		M3	M4	M5		Mode M3 M4 M5				M5				
	]	B linkin	g OFF		L	-	-	L	3b	it data	input		L	L	-		
		Blink 1	Black		H	L	L		16	it data	input		L	H	-		
		Blink			H	н	L	L	4b	it data	input		H	-	-		
	Blink Inversion H - H																
Unassigned bit : No care, it can be H or L (L is Recommended)																	

### 9.5.2 MODE CHART



### 9.6 Timing chart and details of mode

### 9.6.1 SINGLE LINE UPDATE MODE (3bit-data mode)

	Updates data of only one spe	cified line.	]	Mode table M0 M1 H L/H	M2 M3 L L	M4 M5 L -	
scs							
SI SCLI			60 (AG5) (AG4) (AG3) (AG Iness select period (10 cla Gate single line	ίτι		02R X02G X021	
SCS <sup>-</sup>							
SI [		Dummy data					
SCL			<u> </u>	<u>u u u</u>			
	Data write period Gate single line			nsfer period (160 Data transfer	clocks)		

M0 : Mode flag. Set "H", data update mode.

M1 : COM inversion flag. In the case of EXTMODE="L", it is valid.

In the case of "H", outputs COM="H".

In the case of "L", outputs COM="L".

In the case of EXTMODE="H", it is invalid, it can be "H" or "L".

M2 : All clear flag. Set "L", data update mode.

M3-M4 : Data-bit control flag. In the case of M3="L" and M4="L", 3bit-data mode.

M5 : Invalid data, it can be "H" or "L".

AG9-AG0 : Gate line address (10bit), refer to the Gate line address table.

Data : Pixel memory data. In the case of "L", pixel is black.

In the case of 3bit-data mode,

input serially the pixel data in the order of Red-Green-Blue (3bit).

n : Number of horizontal line, refer to the Display address map and Pixel layout.

Dummy data : It can be "H" or "L".

Insert transfer period which is 16clocks after the last data. M0, M2 flags are cleared by SCS="L", and M3-M4 flags are cleared by DISP="L".

9.6.2 MULTIPLE LINES UPDATE MODE (3bit-data mode)								
Updates arbitrary multiple lines data. Mode table								
M0         M1         M2         M3         M4         M5           H         L/H         L         L         L         -								
SCS								
SI								
SCS <sup></sup>								
SI								
SCLK								
Cate 1 <sup>st</sup> line Gate 2 <sup>nd</sup> line								
SCS SI \								
Data write period * Data transfer period (6 clocks) * Gate line address select period (10 clocks) * Data write period Gate (m-1)* line Gate m* line								
scs								
SI X X X X X X X X X X X X X X X X X X X								
SCLK Data write period								
Gate m <sup>±</sup> line Data transfer								
<ul> <li>M0 : Mode flag. Set "H", data update mode.</li> <li>M1 : COM inversion flag. In the case of EXTMODE="L", it is valid.</li> <li>In the case of "H", outputs COM="H".</li> <li>In the case of "L", outputs COM="L".</li> <li>In the case of EXTMODE="H", it is invalid, it can be "H" or "L".</li> <li>M2 : All clear flag. Set "L", data update mode.</li> <li>M3-M4 : Data-bit control flag. In the case of M3="L" and M4="L", 3bit-data mode.</li> <li>M5 : Invalid data, it can be "H" or "L".</li> </ul>								
AG9-AG0 : Gate line address (10bit), refer to the Gate line address table.								
Data : Pixel memory data. In the case of "L", pixel is black. In the case of 3bit-data mode, input serially the pixel data in the order of Red-Green-Blue (3bit). n : Number of horizontal line, refer to the Display address map and Pixel layout.								
Dummy data : It can be "H" or "L".								
Input data continuously. m : Number of vertical line, refer to the Display address map and Pixel layout.								
Insert transfer period which is 6clocks between the gate line and the next gate line. Insert transfer period which is 16clocks after the last data. M0, M2 flags are cleared by SCS="L", and M3-M4 flags are cleared by DISP="L".								

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9.6.3 SINGLE LINE UPDATE MODE (1bit-data mode)
Updates data of only one specified line.M0M1M2M3M4M5HL/HLLH-
SCS
SCS SI
M0 : Mode flag. Set "H", data update mode. M1 : COM inversion flag. In the case of EXTMODE="L", it is valid. In the case of "H", outputs COM="H".

In the case of "L", outputs COM="L".

In the case of EXTMODE="H", it is invalid, it can be "H" or "L".

M2 : All clear flag. Set "L", data update mode.

M3-M4 : Data-bit control flag. In the case of M3="L" and M4="H", 1bit-data mode.

M5 : Invalid data, it can be "H" or "L".

AG9-AG0 : Gate line address (10bit), refer to the Gate line address table.

Data : Pixel memory data. In the case of "L", pixel is black.In the case of 1bit-data mode, input the pixel data "H" or "L" (1bit).Pixel memories of red, green and blue are written the same data.n : Number of horizontal line, refer to the Display address map and Pixel layout.

Dummy data : It can be "H" or "L".

Insert transfer period which is 16clocks after the last data. M0, M2 flags are cleared by SCS="L", and M3-M4 flags are cleared by DISP="L".

9.6.4 MULTIPLE LINES UPDATE MODE (1bit-data mode)
Updates arbitrary multiple lines data.
M0         M1         M2         M3         M4         M5           H         L/H         L         H         -
SCS
SCS SI
SCSSCSSCSSCSSCSSDn-2 \Dn-1 \Dn \Dummy data \AG9\AG9\AG9\AG6\AG5\AG6\AG5\AG4\AG3\AG2\AG1\AG0\D1 \D2 \D3 \D4 \ SCLKSCLKSCLS
SCS <sup></sup> SI <u>(X X Dn-3)Dn-2)Dn1)Dn</u> Dummy data SCLK Data write period <sup>4</sup> Data transfer period (16clocks) Gate m <sup>4</sup> line Data transfer
M0 : Mode flag. Set "H", data update mode. M1 : COM inversion flag. In the case of EXTMODE="L", it is valid. In the case of "H", outputs COM="H". In the case of "L", outputs COM="L". In the case of EXTMODE="H", it is invalid, it can be "H" or "L". M2 : All clear flag. Set "L", data update mode. M3-M4 : Data-bit control flag. In the case of M3="L" and M4="H", 1bit-data mode. M5 : Invalid data, it can be "H" or "L".
AG9-AG0 : Gate line address (10bit), refer to the Gate line address table.
Data : Pixel memory data. In the case of "L", pixel is black. In the case of 1bit-data mode, input the pixel data "H" or "L" (1bit). Pixel memories of red, green and blue are written the same data. n : Number of horizontal line, refer to the Display address map and Pixel layout.
Dummy data : It can be "H" or "L".
Input data continuously. m : Number of vertical line, refer to the Display address map and Pixel layout.

Insert transfer period which is 6clocks between the gate line and the next gate line. Insert transfer period which is 16clocks after the last data.

M0, M2 flags are cleared by SCS="L", and M3-M4 flags are cleared by DISP="L".

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9.6.5 SINGLE LINE UPDATE MOI	DE (4bit-c	data mode)		
Updates data of only one s	specified line	. Mode table M0 M1 M2 M3 M4 M5 H L/H L H		
SCS		AG6)/AG5/AG4/AG3/AG2/AG1/AG0/DIR/D1G/D1B/DUM/D2R/D20 defenses select period (10 clocks) * Data write period Gate single line		- - -
SCS <sup></sup> SI <u>XXXX</u> DuR DuG DuB ( SCLK Data write period Gate single line	DUM Dummy data	Data transfer Data transfer		-
M0 : Mode flag. Set "H", data update M1 : COM inversion flag. In the case In the case of "H", outputs COM="H". In the case of "L", outputs COM="L". In the case of EXTMODE="H", it is inv M2 : All clear flag. Set "L", data updat M3 : Data-bit control flag. In the case M4-M5 : Invalid data, it can be "H" or	of EXTMC valid, it can the mode. of M3="H'	n be "H" or "L".		
AG9-AG0 : Gate line address (10bit),	refer to th	e Gate line address table.		
Data : Pixel memory data. In the case In the case of 4bit-data mode, input serially the pixel data in the orde	-			
Dummy data (DUM) can be "H" or "L" n : Number of horizontal line, refer to		y address map and Pixel layout.		
Dummy data : It can be "H" or "L".				
Insert transfer period which is 16clock M0, M2 flags are cleared by SCS="L"				
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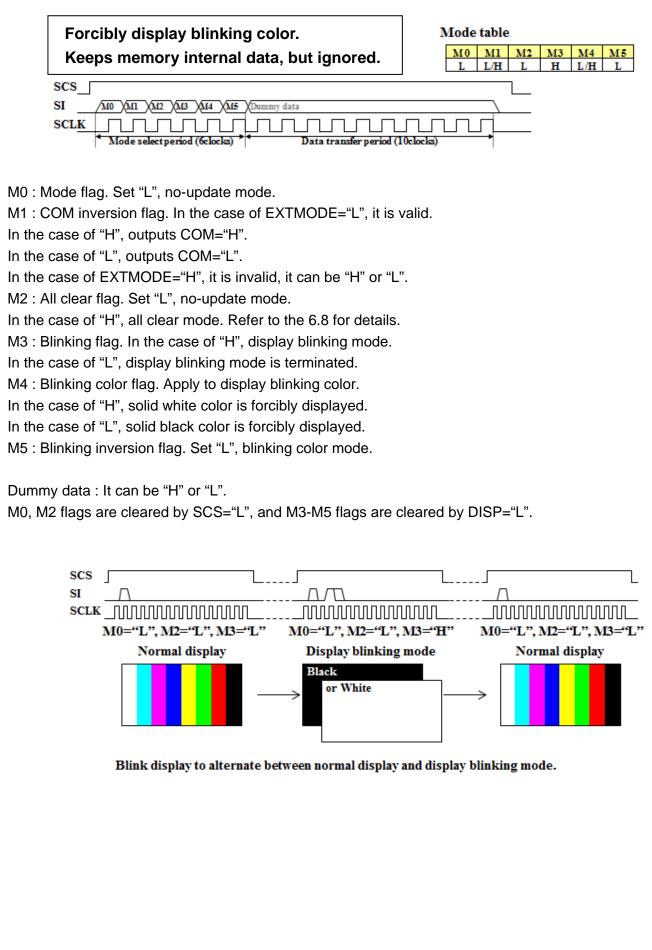
9.7 MULTIPLE LINES UPDATE MODE (4bit-data mode)
Updates arbitrary multiple lines data. Mode table
M0 M1 M2 M3 M4 M5
SCS
SI
SCS
SI
SI
SCS
SI
Gate III- IIIe Data transier
<ul> <li>M0 : Mode flag. Set "H", data update mode.</li> <li>M1 : COM inversion flag. In the case of EXTMODE="L", it is valid.</li> <li>In the case of "H", outputs COM="H".</li> <li>In the case of "L", outputs COM="L".</li> <li>In the case of EXTMODE="H", it is invalid, it can be "H" or "L".</li> <li>M2 : All clear flag. Set "L", data update mode.</li> <li>M3 : Data-bit control flag. In the case of M3="H", 4bit-data mode.</li> <li>M4-M5 : Invalid data, it can be "H" or "L".</li> </ul>
AG9-AG0 : Gate line address (10bit), refer to the Gate line address table.
Data : Pixel memory data. In the case of "L", pixel is black. In the case of 4bit-data mode, input serially the pixel data in the order of Red-Green-Blue-Dummy (4bit). Dummy data (DUM) can be "H" or "L". n : Number of horizontal line, refer to the Display address map and Pixel layout.
Dummy data : It can be "H" or "L".
Input data continuously. m : Number of vertical line, refer to the Display address map and Pixel layout.
Insert transfer period which is 6clocks between the gate line and the next gate line. Insert transfer period which is 16clocks after the last data. M0, M2 flags are cleared by SCS="L", and M3 flag is cleared by DISP="L".

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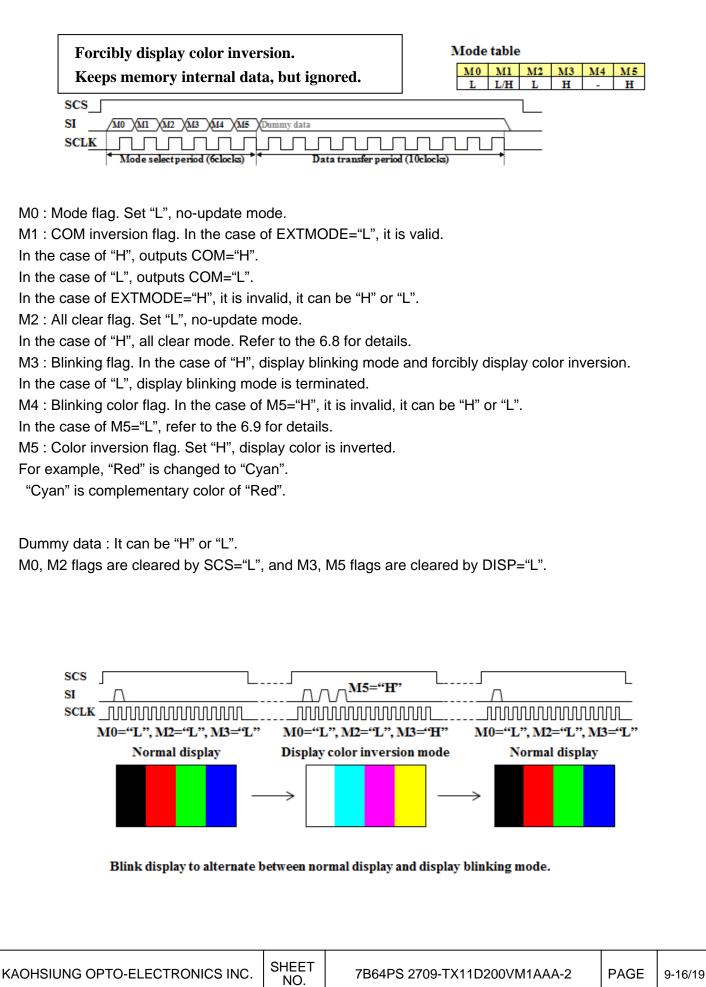
9.8 No-UPDATE MODE							
Keeps memory internal display).	data (cui	rrent	Mode L M0 H	table <u>M1 M</u> L/H L <u>M1 M</u> L/H H	L 2 M3 M	14 M5  14 M5 	
SCS	Dummy data	ta transfer period (10clo			-		
<ul> <li>M0 : Mode flag.</li> <li>M1 : COM inversion flag. In the case of In the case of "H", outputs COM="H".</li> <li>In the case of "L", outputs COM="L".</li> <li>In the case of EXTMODE="H", it is inv</li> <li>M2 : All clear flag.</li> <li>Set "L" or "H" to both M0 and M2, no-to M3 : Blinking flag. In the case of "L", m</li> <li>In the case of "H", display blin</li> <li>M4-M5 : Invalid data, it can be "H" or "</li> </ul>	valid, it car update mo no-update nking mod	n be "H" or "L". ode. mode and displa	ay blinking	-	is termir	ated.	
Dummy data : It can be "H" or "L".							
M0, M2 flags are cleared by SCS="L",	, and M3 f	lag is cleared by	' DISP="L	"			
						1	
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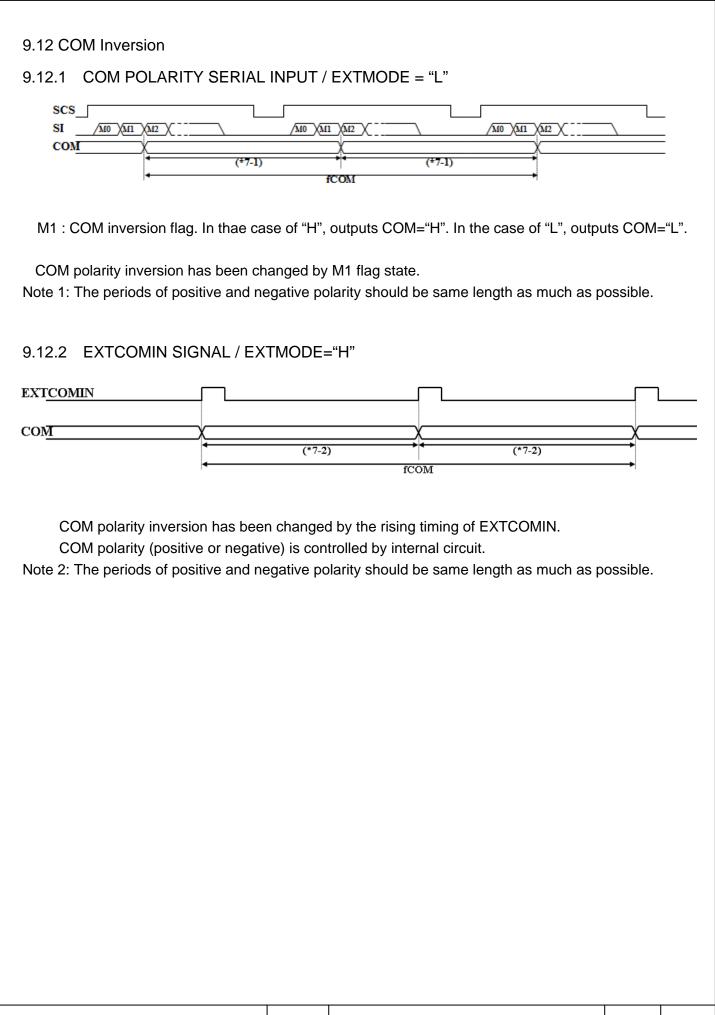
9.9 ALL CLEAR MODE					
Clears memory internal of Initial data is black. SCS	Dummy data	rites initial data.		14 M5 /H L/H	
<ul> <li>M0 : Mode flag. Set "L", no-update models</li> <li>M1 : COM inversion flag. In the case of In the case of "H", outputs COM="H".</li> <li>In the case of "L", outputs COM="L".</li> <li>In the case of EXTMODE="H", it is involved to the case of EXTMODE="H", it is involved to the case of "L", all clear flag. Set "H", all clear models</li> <li>M3 : Blinking flag. In the case of "L", or In the case of "H", display blint</li> <li>M4-M5 : Blinking mode flag. In the case of M3="L", it is involved to the case of M3="L".</li> </ul>	of EXTMC valid, it car ode. display blir hking mod se of M3=	n be "H" or "L". hking mode is ter e. Refer to the 6. "H", it is valid.	minated.		
Dummy data : It can be "H" or "L".					
M0, M2 flags are cleared by SCS="L",	, and M3-I	M4 flags are clea	red by DISP="L".		
Display gives priority to blinking flag (I	M3).				
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### 9.10 DISPLAY BLINKING COLOR MODE



### 9.11 DISPLAY COLOR INVERSION MODE





### 9.13 Gate address table

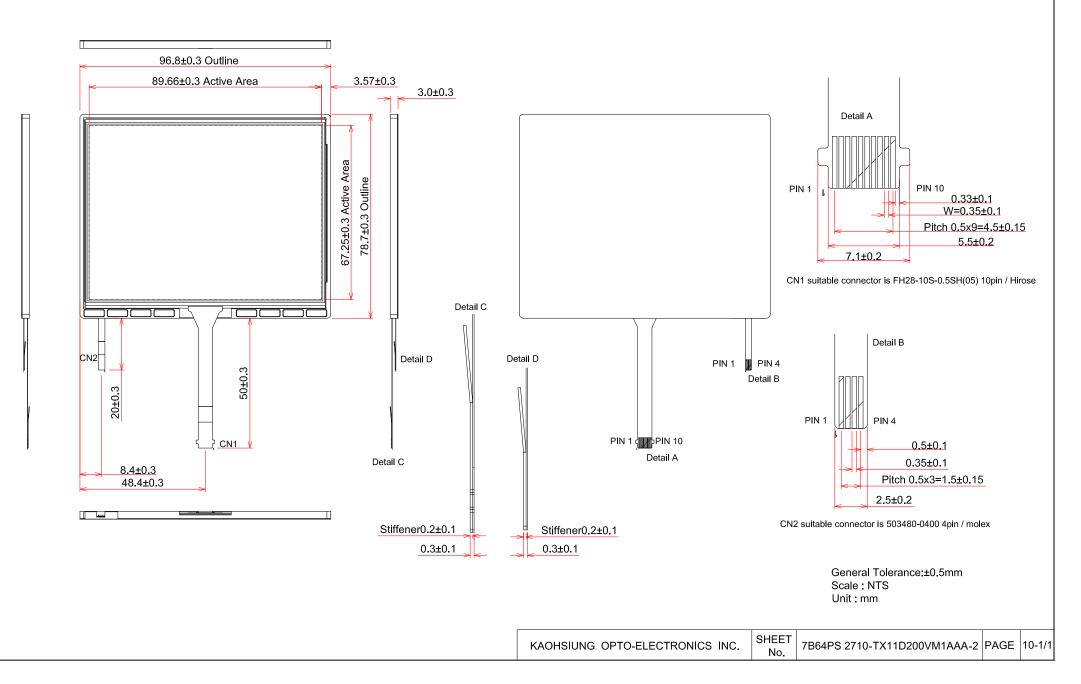
LPM044M141 : V1- V255

	104	410114	ŧı.	V I-	v 200	,																										
	V		G AC 7 6	-		AG AG AG 2 1 0	v	AG 9		G AG 7 6	_	-	AG A0 3 2	-	-	v	AG 9	AG 8	AG / 7	AG AG 6 5		-	AG AG 2 1	AG 0	v		AG A 8 7	G AG	AGA 54		AG AG AG 2 1 0	
	0	0 0	0 0	0	0 0	0 0 0	64	-	-	0 1			0 0		0	128	0	0	1	0 0	0		0 0	0	192		0 1		0 (		0 0 0	
		-	0 0 0 0			$   \begin{array}{c cccccccccccccccccccccccccccccccccc$	65 66	0		0 1		-	0 0 0 0		1 0	129 130	0	0	1	0 0 0 0	0		00 01	1 0	193 194	0	$\begin{array}{c c} 0 & 1 \\ \hline 0 & 1 \end{array}$		0 (		$\begin{array}{c c}0 & 0 & 1\\ \hline 0 & 1 & 0\end{array}$	
			0 0			0 1 1	67	-		0 1			0 0		1	131	0	0	1	0 0	0		0 1	1	195		0 1	1	0 (		0 1 1	
			00 00			100 101	68 69	~	-	0 1 0 1		-	0 1 0 1	-	-	132 133	0	0	1	000			1 0 1 0	0 1	196 197		0 1 0 1		0 (		1 0 0 1 0 1	41
	-		0 0			$\begin{array}{c c} 1 & 0 & 1 \\ \hline 1 & 1 & 0 \end{array}$	70	-		0 1	-	-	$\begin{bmatrix} 0 & 1 \\ 0 & 1 \end{bmatrix}$		0	133	0	0	1	0 0	0		1 1	0	198	-	0 1		0 (		$\begin{array}{c c} 1 & 0 \\ 1 & 1 \\ \end{array}$	
			0 0			1 1 1	71	~		0 1		-	0 1		1	135	0	0	1	0 0	0		1 1	1	199	-	0 1		0 (		1 1 1	
	-		0 0 0 0		-	0 0 0 0 0 1	72 73	~	~	0 1 0 1		-	$   \frac{1}{1}   0 $	-	-	136 137	0	0	1	0 0 0 0	0		0 0 0 0	0 1	200 201	-	0 1 0 1	_	0 (		0 0 0 0 0 1	11
			0 0			0 1 0	74	~	~	0 1			1 0		0	138	0	0	1	0 0	0		0 1	0	202	-	0 1	_	0 (		0 1 0	
			0 0 0 0			$\begin{array}{c c}0 & 1 & 1\\1 & 0 & 0\end{array}$	75 76	0		$\begin{array}{c c} 0 & 1 \\ 0 & 1 \end{array}$	-	0 0	$\begin{array}{c c} 1 & 0 \\ 1 & 1 \end{array}$		1	139 140	0	0	1	0 0 0 0	0	-	$\begin{array}{c c}0 & 1\\1 & 0\end{array}$	1 0	203 204	-	0 1 0 1	1	0 (		$\begin{array}{c c}0 & 1 & 1\\1 & 0 & 0\end{array}$	
	_		0 0	-	-	1 0 1	77		0	0 1		-	1 1	-	-	141	0	0	1	0 0	0		1 0	1	205	0	0 1	1	0 (		1 0 1	
	_	~ ~	00 00		01	1 1 0 $     1 1 1$	78 79	~	~	0 1 0 1		0	$     \begin{array}{c}       1 \\       1 \\       1     \end{array}   $	1	0 1	142 143	0	0	1	000	0	1	1 1 1 1	0 1	206 207	-	0 1 0 1	1	00		$     \begin{array}{c cccccccccccccccccccccccccccccccc$	41
			0 0			$\begin{array}{c c} 1 & 1 \\ 0 & 0 \\ \end{array}$	80		~	0 1	0	-	$\begin{bmatrix} 1 \\ 0 \end{bmatrix}$	_	0	143	0	0	1	0 0	1		0 0	0	207	-	0 1	1	0 1		$\begin{array}{c c} 1 & 1 \\ 0 & 0 \\ \end{array}$	
			0 0			0 0 1	81	0	~	0 1		_	0 0		-	145	0	0	1	0 0			0 0	1	209	-	0 1		0 1	_	0 0 1	]
			0 0 0 0			$     \begin{array}{c cccc}       0 & 1 & 0 \\       0 & 1 & 1 \\     \end{array} $	82 83	-	~	0 1 0 1			00 00		0	146 147	0	0	1	0 0 0 0	1		0 1 0 1	0 1	210 211	-	0 1 0 1	-	0 1 0 1		$     \begin{array}{c cc}       0 & 1 & 0 \\       0 & 1 & 1 \\     \end{array} $	11
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277 0 1	0 0	0 1	_	0 1	_	0 1	341	0	1	0	1	0	1	0	1	0	1	405	0	1	1	0	0		0	-	1	469	0	1	1	1	_	_	0 1	-	1
278 0 1 279 0 1	0 0	0 1		0 1		1 0 1 1	342		1	0	1	0	1	0	1	1	0	406	0	1	1	0	0		0		0	470	0	1	1	1			0 1		0
279         0         1           280         0         1	0 0 0 0	0 1 0 1	_	0 1 1 0	_	1 1 0 0	343 344		1	0	1	0	1	0 1	1	1 0	1 0	407 408	0	1	1	0	0		0 : 1 (	1 ) 0	1 0	471 472	0	1	1	1	_	_	0 1 1 (		1
281 0 1	0 0	0 1				0 1	345		1	0	1	0	1	1	0	0	1	409	0	1	1	0	0			) 0	1	473	0	1	1	1			1 (		1
282 0 1	0 0	0 1		1 0	_	1 0	346		1	0	1	0	1	1	0	1	0	410	0	1	1	0	0		1 (	_	0	474	0	1	1	1			1 (		0
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284         0         1           285         0         1	0 0 0 0	0 1 0 1	-			0 0 0 1	348 349		1	0	1	0	1	1	1	0	0	412 413	0	1	1	0	0		1 : 1 :		0	476 477	0	1	1 1	1			1 1		0
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289         0         1           290         0         1	0 0 0 0	1 ( 1 (		0 0 0 0	_	0 1 1 0	353 354		1	0	1	1 1	0	0	0	0 1	1 0	417 418	0	1	1	0	1		00	) 0 ) 1	1 0	481	0	1	1	1	1	0			0
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294         0         1           295         0         1	0 0 0 0	1 ( 1 (	_	0 1 0 1	_	1 0 1 1	358 359		1	0	1	1	0	0	1	1	0 1	422 423	0	1	1	0	1		0 : 0 :		0	480	0	1	1	1	1	0	0 1	1	1
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304         0         1           305         0         1	0 0 0 0	1		0 0 0 0		0 0 0 1	368 369		1	0	1	1	1	0	0	0	0	432 433	0	1	1	0	1		00		0	490	0	1	1	1	1	1	0 0	0	1
306 0 1	0 0	1 1	-	0 0	-	1 0	370		1	0	1	1	1	0	0	1	0	434	0	1	1	0	1		0		0	498	0	1	1	1	1	1	0 (	1	0
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308         0         1           309         0         1	0 0 0 0	1 1 1 1		0 1 0 1		0 0 0 1	372 373		1	0	1	1	1	0	1	0	0	436 437	0	1	1	0	1		0 : 0 :	L 0 L 0	0	500 501	0	1	1	1	1	1	0 1	0	0
309         0         1           310         0         1	0 0	1			-	1 0	373		1	0	1	1	1	0	1	1	0	437	0	1	1	0	1		0. 0.:	l 0	0	502	0	1	1	1	1	1	0 1	. 1	0
311 0 1	0 0	1 1		0 1		1 1	375		1	0	1	1	1	0	1	1	1	439	0	1	1	0	1		0	1	1	503	0	1	1	1	1	1	0 1	. 1	1
312 0 1	0 0	1 1	1	1 0		0 0	376		1	0	1	1	1	1	0	0	0	440	0	1	1	0	1	1	1 (	_	0	504	0	1	1	1	1	1	1 (	0	0
313         0         1           314         0         1	0 0 0 0	1 1 1 1		1 () 1 ()	_	0 1 1 0	377 378	_	1	0	1	1	1	1	0	0 1	1 0	441 442	0	1	1	0	1	1	1 ( 1 (		1 0	505 506	0	1	1	1	1	1	1 (	0	1
314     0     1       315     0     1	0 0	1				1 1	378		1	0	1	1	1	1	0	1	1	442	0	1	1	0	1	1	1 (		1	507	0	1	1	1	1	± 1	1 (		1
316 0 1	0 0	1 1	1			0 0	380		1	0	1	1	1	1	1	0	0	444	0	1	1	0	1	1	1	1 0	0	508	0	1	1	1	1	1	1 1	. 0	0
317 0 1	0 0	1 1		1 1		0 1	381		1	0	1	1	1	1	1	0	1	445	0	1	1	0	1	1	1	1 0	1	509	0	1	1	1	1	1	1 1	. 0	1
318         0         1           319         0         1	0 0	1 1		1 1 1 1		1 0 1 1	382 383		1	0	1	1	1	1	1	1	0	446 447	0	1	1	0	1	1	1 1		0	510 511	0	1	1	1	1	1	1 1 1 1	. 1	0
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# **10. OUTLINE DIMENSIONS**



# **11. APPEARANCE STANDARD**

The appearance inspection is performed in a room around 500~1000 lx based on the conditions as below:

- The distance between inspector's eyes and display is 30 cm.
- The viewing zone is defined with angle  $\theta$  shown in Fig.11.1 The inspection should be performed within  $45^{\circ}$  when display is shut down. The inspection should be performed within  $5^{\circ}$  when display is power on.

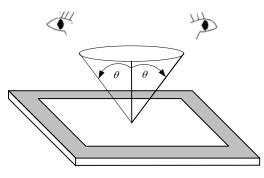


Fig. 11.1

### 11.1 THE DEFINITION OF LCD ZONE

LCD panel is divided into 2 areas as shown in Fig.11.2 for appearance specification in next section. A zone is the LCD active area (dot area); B zone is the area between A zone and LCD edge.

In terms of housing design, B zone is the recommended window area customers' housing should be located in.

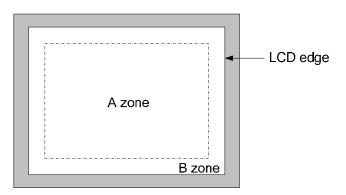


Fig. 11.2

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### 11.2 LCD APPEARANCE SPECIFICATION

The specification as below is defined as the amount of unexpected phenomenon or material in different zones of LCD panel. The definitions of length, width and average diameter using in the table are shown in Fig.11.3 and Fig.11.4.

	Item		Zone						
Dot type	B/W spot	Average Diameter (mm)	Maximum Number	Minimum Space					
	(Dent in glass or	D≦0.15	Ignore	-	А				
	Upper polarizer, Particle, Swell)	0.15 <d≦0.25< td=""><td>2</td><td>-</td><td></td></d≦0.25<>	2	-					
	Bright/Dark dot	0.25 <d< td=""><td>0</td><td>-</td><td></td></d<>	0	-					
	defect	D≦0.25	Ignore	-					
		0.25 <d≦0.3< td=""><td>3</td><td>-</td><td>В</td></d≦0.3<>	3	-	В				
		0.3 <d< td=""><td>0</td><td>-</td><td></td></d<>	0	-					
			С						
		Keep tw							
Line type	Scratch on Upper	Length (mm)	Width (mm)	Maximum Number					
	polarizer or	-	W≦0.03	Ignore	А				
	Foreign material between Upper	L≦2	0.03 <w≦0.08< td=""><td>2</td><td></td></w≦0.08<>	2					
	polarizer and Glass	2 <l< td=""><td>0.08<w< td=""><td>0</td><td></td></w<></td></l<>	0.08 <w< td=""><td>0</td><td></td></w<>	0					
		L≦3	W≦0.10	3	в				
		3 <l< td=""><td>0.10<w< td=""><td>0</td><td>D</td></w<></td></l<>	0.10 <w< td=""><td>0</td><td>D</td></w<>	0	D				
			С						
		Keep two	defect distance m	ore than 5mm					
Air bubble	Air bubble	Average Diameter (mm)	Maximum Number	Minimum Space					
		D≦0.15	Ignore	-	А				
		0.15 <d≦0.25< td=""><td>2</td><td>-</td><td><i>/</i> · ·</td></d≦0.25<>	2	-	<i>/</i> · ·				
		0.25 <d< td=""><td>-</td><td></td></d<>	-						
			В						
		Ignore							

The limitation of glass flaw occurred is defined in the table as below. Item Specifications  $X \leq 3.0 \text{ mm}$  $Y \leq 3.0 \text{ mm}$ Edge flaw  $Z \leq Thickness$  $X \leq 2.0 \text{ mm}$  $Y \leq 2.0 \text{ mm}$ Corner flaw Z ≤ Thickness Not allowed Progressive flaw Length Vidth a+b Average diameter =

Fig.11.3

Fig.11.4

Note 1: C zone defects other than the above are ignored when function / display is not affected.

Note 2: When there is an agreement limit samples, Item is judged according to limit sample.

Note 3: Total defect quantity : A zone (N $\leq$ 3) each inspection (lighting / appearance), B zone (N $\leq$ 5).

Note 4: Other items are to be decided by agreement between both parties.

Note 5: Ignore any dirt which can be removed.

## **12. PRECAUTIONS**

### 12.1 PRECAUTIONS of ESD

- 1) Before handling the display, please ensure your body has been connected to ground to avoid any damages by ESD. Also, do not touch display's interface directly when assembling.
- 2) Please remove the protection film very slowly before turning on the display to avoid generating ESD.

### **12.2 PRECAUTIONS of HANDLING**

- 1) In order to keep the appearance of display in good condition, please do not rub any surfaces of the displays by using sharp tools harder than 3H, especially touch panel, metal frame and polarizer.
- 2) Please do not stack the displays as this may damage the surface. In order to avoid any injuries, please avoid touching the edge of the glass or metal frame and wore gloves during handling.
- 3) Touching the polarizer or terminal pins with bare hand should be avoided to prevent staining and poor electrical contact.
- 4) Do not use any harmful chemicals such as acetone, toluene, and isopropyl alcohol to clean display's surfaces.
- 5) Please use soft cloth or absorbent cotton with ethanol to clean the display by gently wiping. Moreover, when wiping the display, please wipe it by horizontal or vertical direction instead of circling to prevent leaving scars on the display's surface, especially polarizer.
- 6) Please wipe any unknown liquids immediately such as saliva, water or dew on the display to avoid color fading or any permanent damages.
- 7) Maximum pressure to the surface of the display must be less than  $1.96 \times 10^4$  Pa. If the area of applied pressure is less than  $1 \text{ cm}^2$ , the maximum pressure must be less than 1.96N.

### **12.3 PRECAUTIONS OF OPERATING**

- 1) Please input signals and voltages to the displays according to the values defined in the section of electrical characteristics to obtain the best performance. Any voltages over than absolute maximum rating will cause permanent damages to this display. Also, any timing of the signals out of this specification would cause unexpected performance.
- 2) When the display is operating at significant low temperature, the response time will be slower than it at 25 C°. In high temperature, the color will be slightly dark and blue compared to original pattern. However, these are temperature-related phenomenon of LCD and it will not cause permanent damages to the display when used within the operating temperature.
- 3) The use of screen saver or sleep mode is recommended when static images are likely for long periods of time. This is to avoid the possibility of image sticking.
- 4) Spike noise can cause malfunction of the circuit. The recommended limitation of spike noise is no bigger than  $\pm 100$  mV.

NO.

### **12.4 PRECAUTIONS of STORAGE**

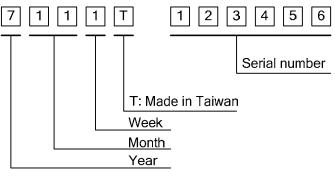
If the displays are going to be stored for years, please be aware the following notices.

- 1) Please store the displays in a dark room to avoid any damages from sunlight and other sources of UV light.
- 2) The recommended long term storage temperature is between 10 C° ~35 C° and 55%~75% humidity to avoid causing bubbles between polarizer and LCD glasses, and polarizer peeling from LCD glasses.
- 3) It would be better to keep the displays in the container, which is shipped from KOE, and do not unpack it.
- 4) Please do not stick any labels on the display surface for a long time, especially on the polarizer.

NO.

# 13. DESIGNATION of LOT MARK

1) The lot mark is showing in Fig.13.1. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.





2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Lot Mark
2017	7
2018	8
2019	9
2020	0
2021	1

Month	Lot Mark	Month	Lot Mark
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sep.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week	Lot Mark	
1~7 days	1	
8~14 days	2	
15~21 days	3	
22~28 days	4	
29~31 days	5	

3) Except letters I and O, revision number will be shown on lot mark and following letters A to Z.

4) The location of the lot mark is on the back of the display shown in Fig. 13.2.

Label example:

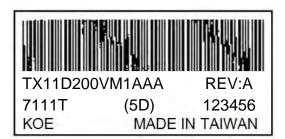


Fig. 13.2